Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 20975

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Third Semester

Electrical and Electronics Engineering

EE 3302 — DIGITAL LOGIC CIRCUITS

(Common to PTEE 3302 for B.E. (Part-Time) First Semester – Regulations 2023)

(Regulations 2021)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State advantages and disadvantages of TTL.
2. Find the octal equivalent of hexadecimal number $(2F.C4)_{16}$.
3. Simplify the given Boolean expression. $(AB + CD) \cdot \left[\left(\overline{A} + \overline{B}\right) \cdot \left(\overline{C} + \overline{D}\right)\right]$.
4. Draw the circuit of the half subtractor and write its truth table.
5. Define race around condition.
6. State the rules for state assignment.
7. What are the drawbacks in designing asynchronous sequential logic circuit?
8. Why the input variables to a PAL buffered?
9. What is data flow modelling in VHDL?
10. Write the VHDL code for a logic gate which gives high output only when both the inputs are high.

PART B — (5 × 13 = 65 marks)

11. (a) (i) How can the expression, Y = (A + B).C be implemented using NAND gates? (5)

(ii) Perform addition for (205+569) using BCD addition. (4)

(iii) Convert the decimal numbers $(31)_{10}$ and $(2,988)_{10}$ into hexadecimal. (4)

Or

(b) (i) Draw the MOS logic circuit for NOT gate and explain its operation. (7)

(ii) Compare Totem pole and Open collector outputs (6)

12. (a) (i) Minimize the fundamental product of sums expression

$$Y = (A + \overline{B} + C) \cdot (\overline{A} + B + C) \cdot (\overline{A} + B + \overline{C}) \cdot (\overline{A} + \overline{B} + C) \cdot (\overline{A} + \overline{B} + \overline{C})$$

first using Boolean algebra and then by using a Karnaugh map. Then draw the circuit which implements the minimized form of Y. (9)

(ii) Simplify the logic function F in the two following cases :

(1) $F(A, B, C) = \min(1, 3, 4, 7)$

(2) $F(A, B, C) = \min(1, 3, 4, 7) + x(2, 5)$, where the don't care terms are represented by x. (4)

Or

(b) (i) Implement the product-of-sums Boolean function expressed by π (1, 2, 5) by a suitable multiplexer. (8)

(ii) Implement the function using decoder

F (p, q, r, s) = $\sum$ (0, 1, 2, 4, 7, 10, 11, 12). (5)

13. (a) For the specified state diagram shown in Figure 1 design a synchronous sequential circuit using D–FF. (13)

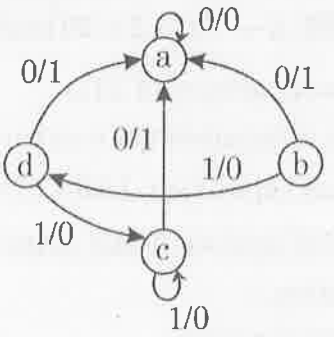

Figure 1

Or

(b) Design a synchronous mod 12 counter using NAND gates and T flip-flops. (13)

14. (a) Analyze the pulse mode circuit shown in figure 2 and derive its flow table. Also plot its state diagram. (13)

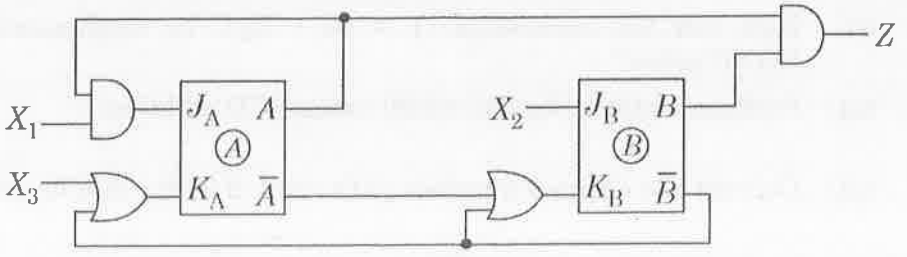

Figure 2

Or

(b) (i) Implement the following using PROM. (9)

$$A(X,Y,Z) = \Sigma_{Max}(1,2,4,6)$$
$$B(X,Y,Z) = \Sigma_{Max}(0,1,6,7)$$
$$C(X,Y,Z) = \Sigma_{Max}(2,6)$$

(ii) What is a Hazard? Brief on its types. (4)

15. (a) (i) Write a VHDL program for 1 to 4 Demux using dataflow modelling. (8)

(ii) Write short notes on built – in operators used in VHDL programming. (5)

Or

(b) Explain in detail the RTL design procedure. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Obtain a set of prime implicants for the Boolean expression. (15)

$f = \Sigma_{Max}$ (0, 1, 6, 7, 8, 9, 13, 14, 15) using a table method.

Or

(b) (i) Design a BCD adder circuit capable of adding BCD equivalents of two-digit decimal numbers. Indicate the IC type numbers used if the design has to be TTL logic family compatible. (11)

(ii) For the given Boolean expression, $Y = \overline{(A \cdot B) + (C \cdot D)}$. Draw the circuit and write the truth-table. (4)